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| 10/699,827 | 11/04/2003 | Kazuhisa Sakihama | 244844US2S | 5577 |

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| EXAMINER | |
|---|---|
| KITOV, ZEEV | |

| ART UNIT | PAPER NUMBER |
|---|---|
| 2836 | |

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Please find below and/or attached an Office communication concerning this application or proceeding.

A12

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 10/699,827 | SAKIHAMA ET AL. | |
| | Examiner | Art Unit | |
| | Zeev Kitov | 2836 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *22 December 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1 - 9, 11, 12, 14 - 18* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1 - 9, 11, 12, 14 - 18* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *04 November 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

## DETAILED ACTION

Examiner acknowledges a submission of the amendment and arguments filed on December 22, 2004. Claims 10 and 13 are deleted; Claims 1, 8, 11, 14 - 17 and 18 are amended. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action.

### *Objection*

Applicant is advised that should claim 5 be found allowable, claim 6 will be objected to under 37 CFR 1.75 as being a substantial duplicate thereof. When two claims in an application are duplicates or else are so close in content that they both cover the same thing, despite a slight difference in wording, it is proper after allowing one claim to object to the other as being a substantial duplicate of the allowed claim. See MPEP § 706.03(k). As a matter of fact, claim 6 is an exact copy of claim 5.

### *Claim Rejections - 35 USC § 102*

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claim 1 - 4 and 16 are rejected under 35 U.S.C. 102(b) as being anticipated by Ma (US 5,841,723). Regarding Claim 1, Ma discloses all the elements of the claim

including a first pad (ground terminal in Fig. 5) used as an external connection terminal to be connected to a semiconductor integrated circuit; a second pad (Vcc terminal in Fig. 5) which is used as an external connection terminal to be connected to the semiconductor integrated circuit; a clamp circuit (element 50 in Fig. 5) connected between the first pad and the second pad; a control circuit (element 44 in Fig. 5) controlling the clamp circuit: and a third pad (PROG terminal in Fig. 5) connected to the control circuit (element 32 in Fig. 5), wherein the control circuit is configured to render the clamp circuit conducting when the same potential as applied to the second pad is applied to the third pad before the semiconductor integrated circuit is incorporated into an end product and to render the clamp circuit non-conducting when a predetermined potential is applied to the third pad after the semiconductor integrated circuit is incorporated into the end product (col. 5, lines 10 – 41).

Regarding Claim 2, Ma discloses the clamp circuit includes a switch element (element 50 in Fig. 5), which is rendered to be conducting or non-conducting in accordance with a control signal output from the control circuit (col. 5, lines 10 – 41).

Regarding Claim 3, Ma discloses the clamp circuit, which includes an inverter circuit (element 44 in Fig. 5) receiving a control signal from the control circuit (element 332 in Fig. 5), and a switch circuit (element 50 in Fig. 5) which is turned on or off by an output signal of the inverter circuit.

Regarding Claim 4, Ma discloses the inverter circuit including a first MOS transistor of a first conductivity type (element 48 in Fig. 5), whose source is connected to the first pad and whose gate is connected to receive the control signal from the

control circuit (element 32 in Fig.5), and a second MOS transistor (element 46 in Fig. 5) of a second conductivity type, whose drain is connected to a drain of the first MOS transistor, whose source is connected to the second pad, and whose gate is connected to receive the control signal from the control circuit.

Regarding Claim 16, Ma discloses the control circuit (element 32 in Fig. 5) including a programmable circuit (elements 20 and 22 in Fig. 5), which renders the clamp circuit conducting before the semiconductor integrated circuit is incorporated into an end product (at the time of manufacturing) and renders the clamp circuit non-conducting after the semiconductor integrated circuit incorporated into an the end product (after manufacturing) (col. 1, line 21 – 34).

### *Claim Rejections - 35 USC § 103*

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 7 and 8 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ma in view of Bishop et al. (US 5,272,371). As was stated above, Ma discloses all the elements of Claims 1 and 3. However, regarding Claim 7, it does not disclose the switch circuit comprises an NPN bipolar transistor. Bishop et al. disclose an NPN bipolar

transistor (element 113 in Fig. 5b) performing clamping function whose collector is connected to the first pad and emitter is connected to the second pad. In Ma reference modified according to Bishop et al. the base of the bipolar is connected to the output of the inverter circuit. Both references have the same problem solving area, namely providing IC protection by clamping. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have further modified the Ma solution by replacing the MOS switch by the NPN bipolar transistor according to Bishop et al., because as Bishop et al. state (col. 3, lines 12 – 14) the bipolar transistors conduction is an effective method of safely conducting charge during an ESD event and additionally, as well known in the art, the parasitic bipolar lateral transistors are readily available as complement to the regular MOS structure; therefore their manufacturing is an easy technological process.

Regarding Claim 8, Bishop et al. disclose the PNP transistor (element 13 in Fig. 1). The motivation for modification of the primary reference is the same as above.

Claim 9 is rejected under 35 U.S.C. 103(a) as being unpatentable over Ma in view of Ker et al. (US 5,959,820) further called Ker 2. 2 As was stated above, Ma discloses all the elements of Claims 1 and 3. However, regarding Claim 9, it does not disclose a switching element as thyristor. Ker 2 discloses the switch circuit including a thyristor (elements NCLSCR1 – NCLSCRn in Fig. 10a) whose anode and cathode are connected between the first pad and the second pad, and a trigger circuit (element 204 in Fig. 10a), which supplies a trigger current to the thyristor to turn on or off the thyristor.

Both references have the same problem solving area, namely providing IC protection by clamping. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have further modified the Ma solution by replacing the MOS transistor by the thyristor according to Ker 2, because as Ker 2 states (col. 1, lines 49 – 55), it has a great bypassing current, which is especially essential for the ESD protecting circuit with limited area.

Claims 5, 6 and 11 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ma in view of Ker 2 and Sedra et al. textbook, Microelectronic Circuits. As was stated above, Ma and Ker 2 disclose all the elements of Claims 1, 3 and 9. However, regarding Claims 5, 6 and 11, it does not disclose the MOS transistor of a second conductivity type. Sedra et al. textbook discloses that MOS transistors exist in two polarity different versions having N amd P channels (NMOS and PMOS) with similar characteristics but having opposite with respect to a power source polarity connections (see pages 344 – 345, Fig. 7.17). As is seen in Fig. 7.17, the N and P channel MOS transistors are mutually replaceable with change of polarity of both input and output signals. Therefore, the circuit consisting of N channel MOS transistor (element 50 in Fig. 5 of Ma) can be modified according to teaching of Sedra et al. by replacing the NMOS with the PMOS. The obtained circuit will have the same electrical characteristics as the one shown in Fig. 5 of Ma, with only exception of required input signal polarity. In such modified circuit to have the same functionality, the inverter should be omitted. Therefore, it would have been obvious to one of ordinary skill in the art at the time the

invention was made to have further modified the Ma solution by changing the NMOS transistor with PMOS transistor in accordance with Sedra et al. teaching, because (I) as Sedra et al. demonstrate, the NMOS and PMOS transistors are mutually replaceable and (II) replacement of NMOS by PMOS would reduce amount of parts. Such decision is a routine task of the designer.

Claims 12 and 14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ma in view of Metz et al. (US 5,400,202). As was stated above, Ma discloses all the elements of Claims 1 and 3. However, regarding Claim 12, it does not disclose the control circuit rendering the clamp circuit conducting when no power is supplied to the semiconductor integrated circuit, and rendering the clamp circuit non-conducting when power is supplied to the semiconductor integrated circuit. Metz et al. disclose the control circuit (elements 42, 40 18 in Fig. 4a, col. 6, line 42 – col. 7, line 9) rendering the clamp circuit conducting when no power is supplied to the semiconductor integrated circuit, and rendering the clamp circuit non-conducting when power is supplied to the semiconductor integrated circuit. Both references have the same problem solving area, namely providing IC protection by clamping. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have further modified the Ma solution by adding the control circuit with features according to Metz et al., because as well known in the art, an integrated circuit can be damaged by an electrostatic discharge from the technician fingers while touching the unpowered integrated circuit.

Regarding Claim 14, Metz et al. disclose a resistor R connected between the gate of the NMOS transistor and to a ground potential to maintain the potential on the gate of the NMOS trigger FET (col. 6, lines 49 – 50). By analogy, similar resistor can be connected between the third pad and a first potential source, i.e. between the gate of transistor 42 in Fig. 4a of Metz et al. and the ground terminal. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have further modified the Ker 1 solution by adding the load circuit (resistor) to the third pad according to Metz et al., because according to Metz et al. (col. 6, lines 49 – 50), such load (resistor) is necessary to maintain the potential on the gate of the NMOS FET; such load resistor will prevent the MOS transistor connected to the third pad from inadvertent turning on.

Claim 15 is rejected under 35 U.S.C. 103(a) as being unpatentable over Ma in view of Metz et al. and further in view of Court Decision *St. Regis Paper Co. v. Bemis Co.,* 193 USPQ 8. As was stated above, Ma and Metz et al. disclose all the elements of Claims 1 and 14. However, regarding Claim 15, they do not disclose a second resistor. The Court Decision addresses this issue by stating that mere duplication of the essential working parts of a device involves only routine skill in the art. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have further modified the Ker 1 solution by adding the second resistor, since it has been held that mere duplication of the essential working parts of a device involves only routine skill in the art.

Claims 16 and 17 is rejected under 35 U.S.C. 103(a) as being unpatentable over Ma in view of Lee et al. (US 6,365,938). As was stated above, Ma discloses all the elements of Claims 1 and 16. However, regarding Claim 17, it does not disclose the programmable circuit having a fuse element. Lee et al. disclose the programmable circuit having the fuse element (elements h in Fig. 5 and 7, col. 6, lines 14 - 28) that is cut after the semiconductor chip is incorporated into the end product, and the semiconductor chip has fourth and fifth pads (end points 7 and 7' on the line 126a in Fig. 5), which supply a current to the fuse element to cut the fuse element after the semiconductor chip incorporated into the end product. Both references have the same problem solving area, namely providing IC protection by clamping. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have further modified the Ma solution by adding the fuse structure according to Lee et al., because as Lee et al. state (col. 1, lines 39 – 48), such structure is necessary for the plasma processing step only and for normal functioning afterwards should be removed.

Claim 18 is rejected under 35 U.S.C. 103(a) as being unpatentable over Ma in view of Lee et al. and Nguen (US 5,682,049). As was stated above, Ma and Lee et al. disclose all the elements of Claims 1 and 16. However, regarding Claim 18, they do not disclose third and fourth resistors. Nguen discloses the fuse circuit (elements 66 and 65 in Fig. 4) including the first resistor (elements R3 and R0 in Fig. 4) connected between the fuse element and a first potential source, i.e. emitter of transistor (element 61 in Fig.

4) and the second resistor (element R2 in Fig. 4) connected between the other end of the fuse element and a second potential, i.e. ground potential. Both references have the same problem solving area, namely adjusting the resistance and voltage values by using fuses. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have further modified the Ma solution by adding the first and the second resistors according to Nguen, because trimming an electrical value potential according to Nguen would adjust the threshold value of the Ma system modified according to Lee et al. to a proper functioning level. Such adjustment of the threshold is necessary to meet demands of different customers, which have different values of the supply voltage and therefore need different threshold values of protection mechanism.

***Response to Arguments***

1. The Applicant's Arguments regarding Ker 1 reference are now moot in view of new ground of rejection.

2. Applicant arguments regarding Metz reference emphasizing functional differences between Metz circuit and the invented circuit sound convincing from engineering standpoint. However, in response to Applicant's Argument that the reference fail to show certain features of the Applicant's invention, it is noted that features upon which Applicant relies, i.e. that functionality of the invented circuit is different from the functionality of the circuit in the reference, are not recited in the rejected Claims. Although the Claims are interpreted in light of the Specification,

limitations from Specification are not read into Claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993).

***Conclusion***

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Zeev Kitov whose current telephone number is (571) 272 - 2052. The examiner can normally be reached on 8:00 – 4:30. If attempts to reach examiner by telephone are unsuccessful, the examiner's supervisor, Brian Sircus can

be reached on (571) 272 – 2800, Ext. 36. The fax phone number for organization where this application or proceedings is assigned is (703) 872-9306 for all communications.

Z.K.
03/18/2005

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